CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device, comprising:

a CAM array that includes a plurality of rows of CAM cells each coupled to a match line;

a priority encoder coupled to the match lines to generate an index;

a counter; and

compare logic coupled to the counter and the priority encoder to compare the index and a counter value from the counter.

2. The CAM device of claim 1, wherein the counter is an address counter.

3. The CAM device of claim 1, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value.

4. The CAM device of claim 3, wherein the address logic comprises a decoder.

5. The CAM device of claim 3, further comprising a multiplexer coupled to the counter and the address logic to selectively output the count value or an input address for the address logic.

6. The CAM device of claim 5, wherein the multiplexer is further coupled to the priority encoder to receive the index.

7. The CAM device of claim 3, further comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device.

8. The CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or an input search key for the CAM array.

9. The CAM device of claim 3, further comprising a multiplexer coupled to the counter to selectively output the counter value or input data for the CAM array.

10. The CAM device of claim 1, further comprising:

a write circuit coupled to the CAM array; and

a comparand register coupled to the CAM array, the comparand register for storing a search key.

11. A content addressable memory (CAM) device, comprising:

a counter; and

a CAM array having a plurality of rows of CAM cells coupled to the counter to receive a counter value as a search key for the CAM array.

12. The CAM device of claim 11, further comprising:

a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells and to generate an index; and

compare logic coupled to the counter and the priority encoder to compare the index and the counter value.

13. The CAM device of claim 12, further comprising address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value.

14. The CAM device of claim 13, further comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device.

15. A content addressable memory (CAM) device, comprising:

a counter;

a CAM array having a plurality of rows of CAM cells coupled to the counter to receive a counter value for storage in at least one of the rows of the CAM cells; and

address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value.

16. The CAM device of claim 15, further comprising:

a priority encoder coupled to receive a plurality of match signals from the plurality of rows of CAM cells and to generate an index; and

compare logic coupled to the counter and the priority encoder to compare the index and the counter value.

17. The CAM device of claim 16, further comprising an instruction decoder coupled to the address logic and adapted to decode instructions received by the CAM device.

18. A content addressable memory (CAM) device, comprising:

a CAM array that includes a plurality of rows of CAM cells each coupled to a match line;

means for determining an index that indicates a location in the CAM array of one of the rows of CAM cells;

means for generating an address of one of the rows of CAM cells in the CAM array; and

means for determining that the address matches the index.

19. A test system, comprising:

a tester that generates test signals; and

a content addressable memory (CAM) device coupled to the tester to receive the test signals, wherein the CAM device comprises:

a CAM array that includes a plurality of rows of CAM cells each coupled to a match line;

a priority encoder coupled to the match lines to generate an index;

a counter; and

a compare logic coupled to the counter and the priority encoder to compare the index and a counter value from the counter.

20. The test system of claim 19, wherein the compare logic has an output coupled to the tester to provide an indication of the comparison between the index and the counter value.

21. The test system of claim 20, wherein the CAM device further comprises address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value.

22. The test system of claim 21, wherein the CAM device further comprises an instruction decoder coupled to the address logic, and wherein the test signals include instructions for the CAM device, and where the instruction decoder is adapted to decode the instructions transmitted to the CAM device.

23. The test system of claim 19, wherein the tester comprises automated test equipment (ATE).

24. The test system of claim 19, wherein the tester comprises a processor.

25. A test system, comprising:

a tester that generates test signals;

a counter that generates a counter value; and

a compare logic coupled to the counter; and

a content addressable memory (CAM) device coupled to the tester to receive the test signals, wherein the CAM device comprises:

a CAM array that includes a plurality of rows of CAM cells each coupled to a match line; and

a priority encoder coupled to the match lines to generate an index, wherein the compare logic is coupled to the priority encoder to compare the index and the counter value.

26. The test system of claim 25, wherein the compare logic has an output coupled to the tester to provide an indication of the comparison between the index and the counter value.

27. The test system of claim 25, wherein the CAM device further comprises address logic coupled to the counter and the CAM array to select at least one of the rows of CAM cells in the CAM array in response to the counter value.

28. The test system of claim 25, wherein the CAM device further comprises an instruction decoder coupled to the address logic, and wherein the test signals include instructions for the CAM device, and where the instruction decoder is adapted to decode the instructions transmitted to the CAM device.

29. A method for operating a content addressable memory (CAM) device, comprising:

systematically identifying locations in a CAM array of the CAM device that store data that match search keys; and

synchronizing a counter within the CAM device with the identifying such that the identifications of the locations match counter values of the counter when the CAM device is operating properly.

30. The method of claim 29, wherein the identifying comprises:

comparing the search keys with the date stored in the CAM array; and

generating indices of the CAM array for the locations that store data that matches the search keys.

31. The method of claim 29, further comprising comparing the indices with the counter values.

32. A method for operating a content addressable memory (CAM) device, comprising:

comparing a search key with data stored in a plurality of rows of CAM cells;

generating an index of a location in the plurality of rows of CAM cells that indicates a match with the search key; and

comparing the index with a first counter value from a counter.

33. The method of claim 32, wherein the data is the same for each of the rows of CAM cells.

34. The method of claim 33, further comprising:

masking CAM cells in a first of the rows of CAM cells corresponding to the first counter value; and

identifying whether the index matches the first counter value.

35. The method of claim 34, further comprising:

unmasking the first row of CAM cells; and

incrementing the counter to a second count value.

36. The method of claim 35, further comprising:

masking CAM cells in a second row of the CAM cells correspond to the second counter value;

repeating the steps of claim 1; and

identifying whether the index matches the second counter value.

37. The method of claim 33, further comprising:

identifying whether the index matches the first counter value;

invalidating the row of CAM cells that stores the first value; and

incrementing the counter to a second counter value.

38. The method of claim 37, further comprising:

repeating the steps of claim 1;

identifying whether the index matches the second counter value; and

invalidating the row of CAM cells that stores the first value.

39. The method of claim 32, further comprising writing, prior to the first comparing step, a unique value to each of the rows of CAM cells such that a first row of the CAM cells having an address corresponding to the first counter value stores the first counter value, and a second row of the CAM cells having an address corresponding to a second counter value stores a second counter value.

40. The method of claim 39, wherein the search key is the first count value.

41. The method of claim 40, further comprising incrementing the counter to the second counter value.

42. The method of claim 41, further comprising:

comparing the second counter value with the data stored in the rows of CAM cells;

generating another index of another location in the plurality of rows of CAM cells that stores the second counter value; and

comparing the another index with the second counter value.

43. A computer-readable medium having stored thereon sequence of instructions, the sequences of instructions including instructions which, when executed by a processor, causes the processor to perform the step of:

systematically identifying locations in a CAM array of the CAM device that store data that match search keys; and

synchronizing a counter within the CAM device with the identifying such that the identifications of the locations match counter values of the counter when the CAM device is operating properly.